CHAPTER 1

Introduction to printed circuit board design and computer-aided design

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Computer-aided design and the OrCAD design suite

Before digging into the details of PCB Editor, we take a moment to discuss computer-aided engineering (CAE) tools in general. CAE tools cover all aspects of engineering design from drawings to analysis to manufacturing. Computer-aided design (CAD) is a category of CAE related to the physical layout and drawing development of a system design. CAD programs specific to the electronics industry are known as electronic CAD or electronic design automation (EDA). EDA tools reduce development time and cost because they allow designs to be simulated and analyzed prior to purchasing and manufacturing hardware. Once a design has been proven through drawings, simulations, and analysis, the system can be manufactured. Applications used in manufacturing are known as computer-aided manufacturing (CAM) tools. CAM tools use software programs and design data (generated by the CAE tools) to control automated manufacturing machinery to turn a design concept into reality.

So how does OrCAD®/Cadence fit into all of this? Cadence owns and manages many types of CAD/CAM products related to the electronics industry, including the OrCAD design suite. The OrCAD design suite can be purchased through resellers

Complete PCB Design Using OrCAD® Capture and PCB Editor
DOI: https://doi.org/10.1016/B978-0-12-817684-9.00001-1

(a list of resellers can be found on the OrCAD.com website), which packages different combinations of CAD/CAM applications, including Capture, PSpice, and PCB Editor, to suit customers' needs. Although these applications can operate individually, bundling the individual tools into one suite allows for intertool communication.

Capture is the centerpiece of the package and acts as the prime EDA tool. Capture contains extensive parts libraries that may be used to generate schematics that stand alone or interact with PSpice, PCB Editor, or both simultaneously. A representation of a Capture part is shown in Fig. 1.1.

The pins on a Capture part can be mapped into the pins of a PSpice model or the pins of a physical package in PCB Editor. PSpice is a CAE tool that contains the mathematical models for performing simulations, and PCB Editor is a CAD tool that converts a symbolic schematic diagram into a physical representation of the design. Netlists are used to interconnect parts within a design and connect each of the parts with its model and footprint. In addition to being a CAD tool, PCB Editor also functions as a front-end CAM tool by generating the data on which other CAM tools operate when manufacturing the PCB. Combining all three applications into one package produces a powerful set of tools to efficiently design, test, and build electronic circuits. The key to successful project design and production is in understanding the PCB itself and knowing how to use the tools that build the PCB.

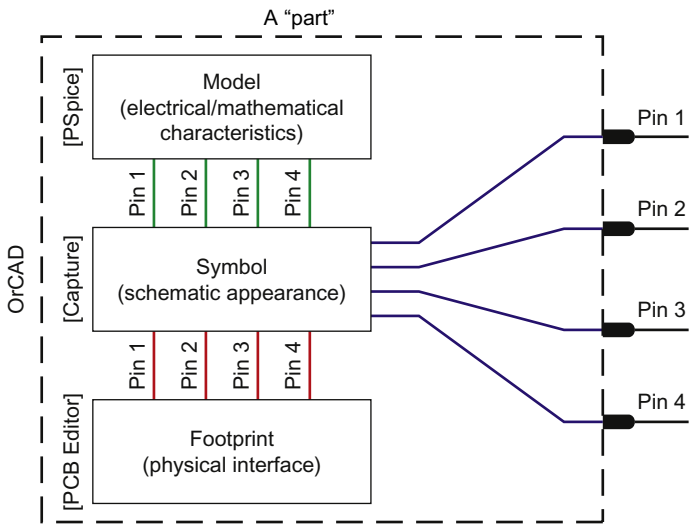

Figure 1.1 The pieces of a "part."

Printed circuit board fabrication

We now look at how PCBs are manufactured for a better understanding of what we are trying to accomplish with PCB Editor and why. A PCB consists of two basic parts: a substrate (the board) and printed wires (the copper traces). The substrate provides a structure that physically holds the circuit components and printed wires in place and provides electrical insulation between conductive parts. A common type of substrate is FR4, which is a fiberglass/epoxy laminate. It is similar to older types of fiberglass boards but is flame resistant. Substrates are also made from Teflon, ceramics, and special polymers.

Printed circuit board cores and layer stack-up

During manufacturing the PCB starts out as a copper clad substrate as shown in Fig. 1.2.

A rigid substrate is a C-stage laminate (fully cured epoxy). The copper cladding may be copper-plated onto the substrate or copper foil glued to the substrate. The thickness of the copper is measured in ounces of copper per square foot, where 1.0 oz/ft^2 of copper is approximately 1.2−1.4 mil (0.0012−0.0014 in. / 0.03−0.035 mm) thick. It is common to drop "/ft^2" and refer to the thickness only in oz. For example, you can order 1 oz copper on a 0.125-in.-thick FR4 substrate.

A substrate can have copper on one or both sides. Multilayer boards are made up of one or more single- or double-sided substrates called *cores*. A core is a copper-plated epoxy laminate. The cores are glued together with one or more sheets of a partially cured epoxy, as shown in Fig. 1.3.

The sheets are also referred to as *prepreg* or *B-stage laminate*. Once all of the cores are patterned (described next) and aligned, the entire assembly is fully cured in a heated press.

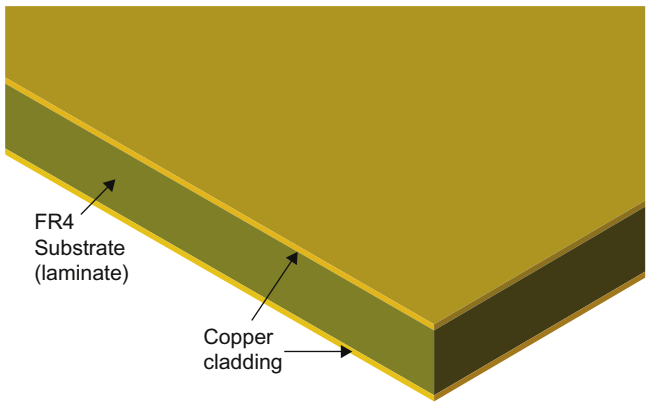

Figure 1.2 A double-sided copper clad FR4 substrate.

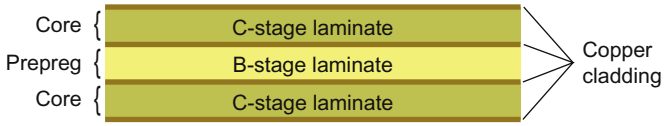

Figure 1.3 Cores and prepreg.

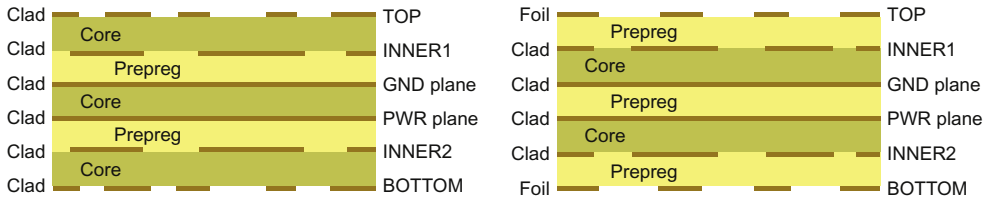

Figure 1.4 Two stack-up methods for a six-layer board: left, multicore, outer clad; right, multicore, outer foil.

There are three methods of assembling the cores when making a multilayer board. Fig. 1.4 shows the first two methods in an example with four routing layers and two plane layers. Fig. 1.4 (left) shows three (double-sided) cores bonded together by two prepreg layers, while Fig. 1.4 (right) shows the same six layers made of two cores, which make up the four inner layers, bonded together by one prepreg layer. The outer layers in this panel are copper foil sheets bonded to the assembly with prepreg.

The routing layers in Fig. 1.4 are shown as patterned copper segments, and the plane layers are shown as solid lines. The inner layers are patterned prior to bonding the cores together. The outer layers are patterned later in the process, after the cores have been bonded and cured and most of the holes have been drilled. Because the outer layers are etched later and copper foil is typically less expensive than copper cladding, the stack-up shown in Fig. 1.4 (right) is more widely used.

The third method uses several fabrication techniques by which highly complex boards can be fabricated, as illustrated in Fig. 1.5. This circuit board may have a typical four-layer core stack-up at its center, but additional layers are built up layer by layer on the top and the bottom, using sequential lamination techniques. The techniques can be used to produce blind and buried vias as well as typical plated through-hole vias, nonplated holes, and back-drilled plated through holes. Resistors and capacitors can also be embedded into the substrate. More about blind vias is discussed in later chapters (Chapter 8: Making and editing footprints and Chapter 9: Printed circuit board design examples).

Printed circuit board fabrication process

The copper traces and pads seen on a PCB are produced by selectively removing the copper cladding and foil. Two methods are commonly used for removing the

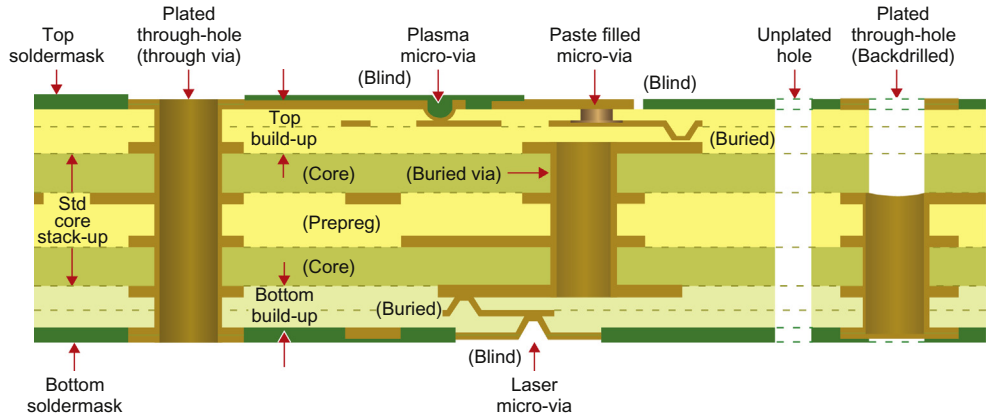

Figure 1.5 A built-up, multitechnology, PCB stack-up. *PCB*, Printed circuit board.

unwanted copper: wet acid etching and mechanical milling. Acid etching is more common when manufacturing large quantities of boards because many boards can be made simultaneously. One drawback to wet etching is that the chemicals are hazardous and must be replenished occasionally, and the depleted chemicals must be recycled or discarded. Milling is usually used for smaller production runs and prototype boards. During milling the traces and pads are formed by a rotating bit that grinds the unwanted copper from the substrate. With either method a digital map is made of the copper patterns. The purpose of CAD software like OrCAD PCB Editor is to generate the digital maps.

Note: Only one layer is considered in the following explanation of the fabrication process.

Photolithography and chemical etching

Selectively removing the copper with etching processes requires etching the unwanted copper while protecting the wanted copper from the etchant. This protection is provided by a polymer coating (called *photoresist*) deposited onto the surface of the copper cladding, as shown in Fig. 1.6.

The photoresist is patterned into the shape of the desired printed circuit through a process called *photolithography*. The patterned resist protects selected areas of the copper from the etchant and exposes the copper to be etched.

The two steps to photolithography are patterning the photoresist and developing it. Patterning is accomplished by exposing the resist to light [typically ultraviolet (UV)], and developing it is accomplished by washing it in a chemical bath. The two types of photoresist are positive resist and negative resist. When positive resist is exposed to UV light, the polymer breaks down and can be removed from the copper. Conversely, negative resist shielded from UV light is removed.

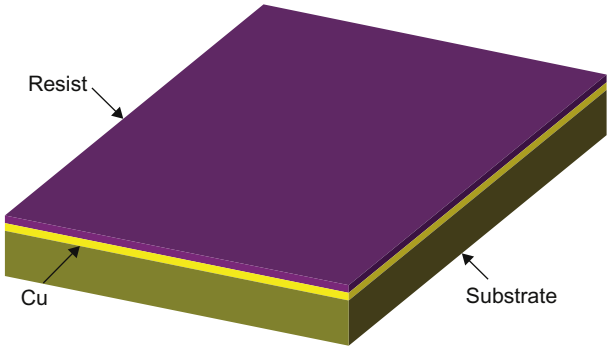

Figure 1.6 A copper clad board coated with photoresist.

A mask is used to expose the desired part of the photoresist. A mask is a specialized black-and-white photographic film or glass photoplate on which a picture of the traces and pads is printed with a laser photoplotter. Two types of masks are shown in Fig. 1.7.

The masks are examples of a trace connected to a pad. Fig. 1.7 (left) shows a positive mask used to expose positive photoresist, and Fig. 1.7 (right) shows a negative mask used to expose negative photoresist. Masks that will be used repeatedly are sometimes produced on glass photoplates instead of film.

The mask is placed on top of the photoresist, as shown in Fig. 1.8, and the assembly is exposed to the UV light. The dark areas block UV light and the white (transparent) areas allow the UV light to hit the photoresist, which imprints the circuit image into the photoresist. A separate mask is used for each layer of a circuit board. OrCAD PCB Editor generates the data that the photoplotter uses to make these masks.

Another way of exposing the photoresist is by using a programmable laser to "draw" the pattern directly onto the photoresist. This is a newer technique, called *laser direct imaging* (LDI). A benefit of the LDI process is that it uses the same data as the photoplotters but no masks are required.

After the photoresist has been exposed (either with the mask and UV or with the laser), it is washed in a chemical called the *developer*. In the case of positive resist the resist breaks down during exposure and is removed by the developer. In the case of negative resist the UV light cures the resist, and only the unexposed resist is removed by the developer. Common developers are sodium hydroxide (NaOH) for positive resist and sodium carbonate (Na_2CO_3) for negative resist. Once the resist has been exposed and developed, a circuit image made of the photoresist is left on the copper, as shown in Fig. 1.9.

Next, the board is etched in a corrosive solution, such as alkaline ammonia or cupric chloride. The etching solution does not significantly affect the photoresist but

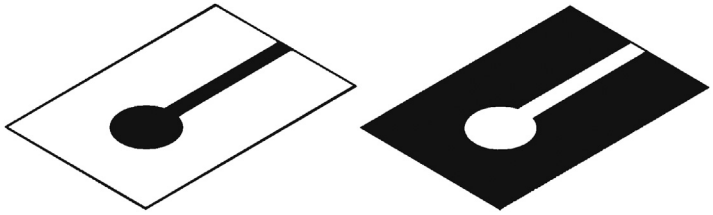

Figure 1.7 Photolithography masks: (left) positive mask and (right) negative mask.

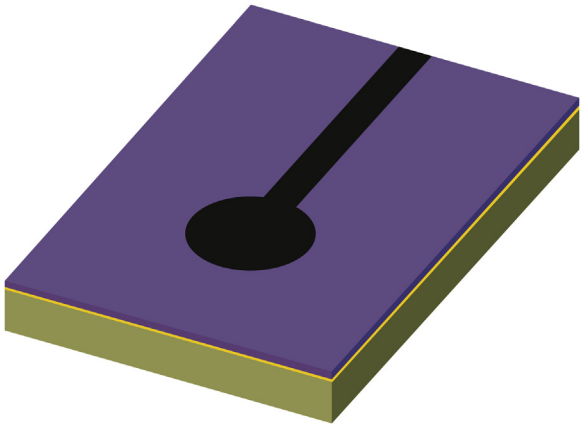

Figure 1.8 Positive photomask on photoresist-coated board.

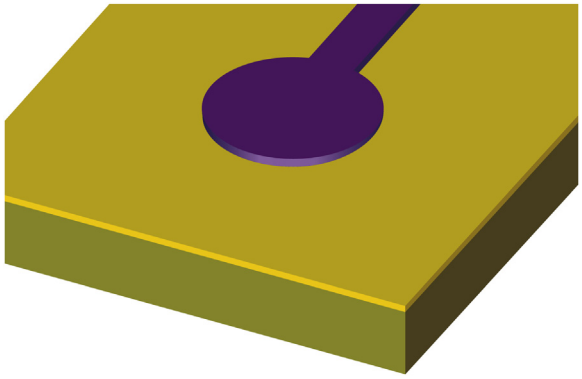

Figure 1.9 Developed photoresist on copper.

attacks the bare copper and removes it from the substrate, leaving behind the resist-coated copper, as shown in Fig. 1.10.

Some processes use a plated tin alloy as the etch resist. The tin alloy plating is more resistant to etchants and preprepares the copper surface for solder processes.

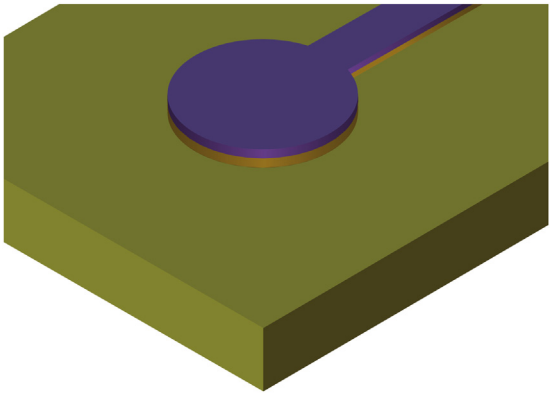

Figure 1.10 Unwanted copper removed by etching.

In this case, photolithography processes are used to selectively plate the circuit pattern onto the copper surfaces prior to etching.

When polymer etch resists are used, the photoresist is cleaned from the copper with a resist stripper, leaving behind the copper traces. Fig. 1.11 shows the final patterned copper. When metal etch resists are used, the plating is typically left in place. Holes for the leads and so forth are not etched into the pads because they are drilled after all of the cores have been glued together (later in the process) to ensure proper alignment of the holes between board layers.

Mechanical milling

As mentioned previously, milling is an alternative to etching. To mill the board a computer numerical control (CNC) machine is programmed with the digital map of the board and grinds away the unwanted copper. The unwanted copper can be completely removed (like that in Fig. 1.11), or just enough copper may be removed to isolate the pads and traces from the bulk copper, as shown in Fig. 1.12. Removing only enough copper to isolate the traces from the bulk copper reduces milling time but can affect the impedance of the traces.

Layer registration

After the inner layers have been patterned, the cores are aligned (called *registration*) and glued together. Registration is critical because the pads on each layer need to be properly aligned when the holes are drilled. Registration is accomplished using alignment patterns (called *fiducials*) and tooling holes in the board, which slide onto guide pins. With the cores in place and properly aligned a heated press cures the assembly.

After the assembly is cured, holes are drilled for through-hole component leads and vias. The drilling process inevitably heats the laminate due to friction between the

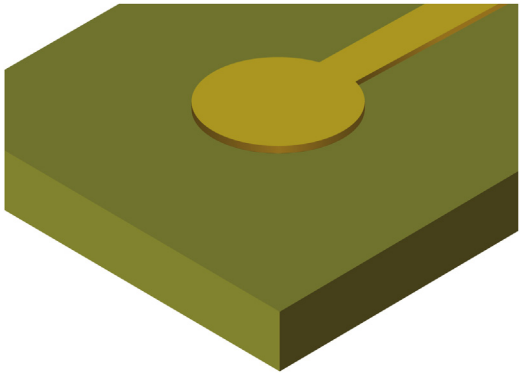

Figure 1.11 Copper pad and trace after etching and resist stripping.

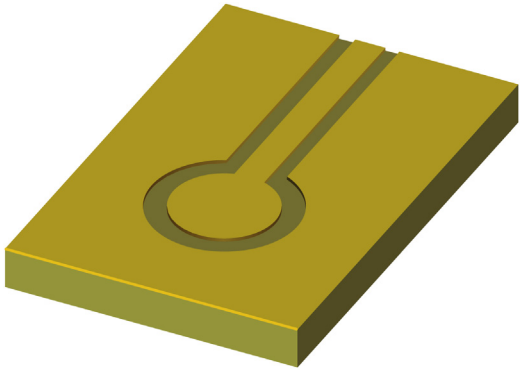

Figure 1.12 A mechanically milled trace.

laminate and the high-speed drill bit. This tends to soften the laminate and smear it across the walls of the drilled copper. After the drilling processes are finished the assembly is placed into a bath to etch back the laminate slightly and clean the faces of the copper pad walls. This is called *laminate etchback* or *desmear*.

Once the holes have been drilled and desmeared, a physical path exists between pads on different layers, but as Fig. 1.13 (left) shows, there is no electrical connection between them. To make electrical connections between pads on different layers the board is placed into a plating bath that coats the insides of the holes with copper, which electrically connects the pads, hence the term *plated* through holes. The plating thickness varies but is typically about 1 mil (0.001 in.) thick. The cutaway view of Fig. 1.13 (right) shows a plated through hole on an internal layer of a PCB. The top and bottom copper is actually patterned *after* the plating process is finished because the plating process would replate the areas where copper had been removed.

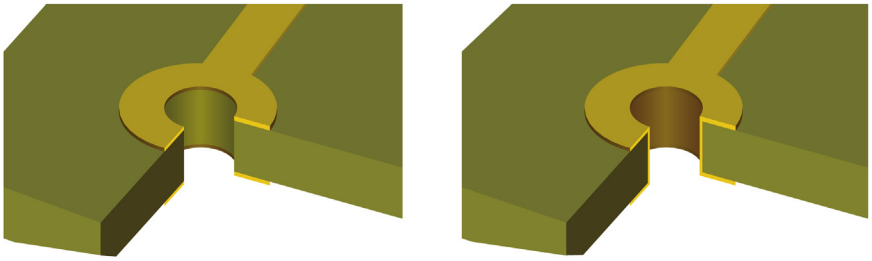

Figure 1.13 Holes are drilled into the board and copper plated: (left) a nonplated through hole and (right) a plated through hole.

Not all layers have traces. Some layers are planes (Fig. 1.14). Plane layers are typically used to provide low-impedance (resistance and inductance) connections to power and ground and to provide easy access to power and ground at any location on the board. Plane layers and impedance issues are discussed in Chapter 6, Printed circuit board design for signal integrity. The leads of components are connected to ground or power by soldering them into plated through holes. Since copper conducts heat well, soldering to a plane layer could require an excessive amount of heat, which could damage the components or the plating in the hole (called the *barrel*). Thermal reliefs are used, as shown in Fig. 1.14, to reduce the path for heat conduction but maintain electrical continuity with the plane.

Since ground and power planes are often inner layers and signal layers will likely be above and below them, in some instances, a via will run through a plane layer but must not touch it. In this case a "clearance" area (shown in Fig. 1.15) is etched into the plane layer around the via to prevent a connection to the plane. The clearance is larger than the normal pad size to ensure that the plane stays isolated from the plated hole.

After the through holes are plated the top and bottom layers are patterned using the photolithography process as described for the inner layers. After the outer copper has been patterned the exposed traces and plated through holes can be tinned (although tinning is sometimes deferred until later). Nonplated holes (such as for mounting holes) may be drilled at this time.

Next, a thin polymer layer is usually applied to the top and bottom of the board. This layer [shown in *dark green* (dark gray in print version) in Fig. 1.16] is called the *soldermask* or *solder resist*. Holes are opened into the polymer using photolithography to expose the pads and holes where components will be soldered to the board. The soldermask protects the top and bottom copper from oxidation and helps prevent solder bridges from forming between closely spaced pads. Sometimes openings in the soldermask are not made over small or densely placed vias (called *tenting a via*). Tented vias are protected from having chemicals such as flux from becoming trapped inside

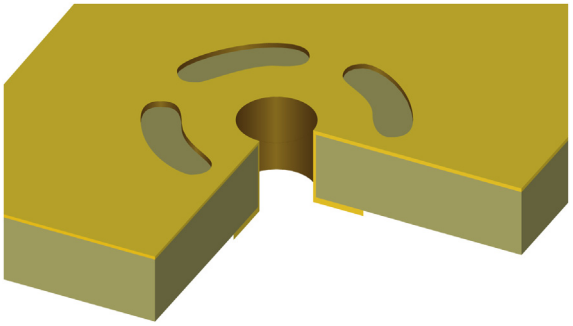

Figure 1.14 A connection to a plane layer through a thermal relief.

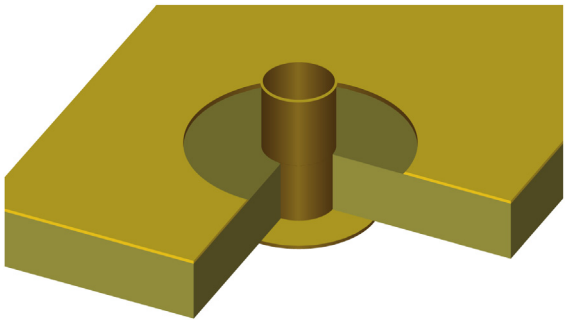

Figure 1.15 A clearance area provides isolation between a plated hole and a plane.

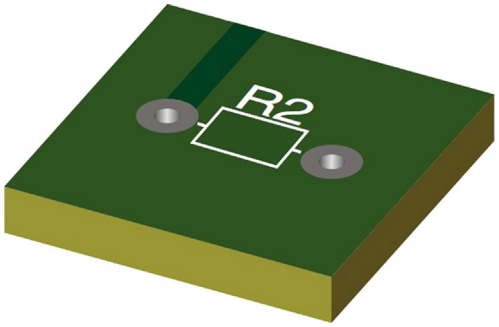

Figure 1.16 Final layers are the soldermask [*dark green* (dark gray in print version)] and silk screen (*white*).

the hole. Tenting also prevents solder migration into the hole, which could lead to poor solder joints on small components that are close to and connected to the via.

Finally, markings (called the *silk screen*) are placed on the board to identify where the components are to be placed. The silk screen is shown in *white* in Fig. 1.16.

Function of OrCAD PCB Editor in the printed circuit board design process

PCB Editor is used to design the PCB by generating a digital description of the board layers for photoplotters and CNC machines, which are used to manufacture the boards. Separate layers are used for routing copper traces on the top, bottom, and all inner layers; drill hole sizes and locations; soldermasks; silk screens; solder paste; part placement; and board dimensions. These layers are not all portrayed identically in PCB Editor. Some of the layers are shown from a positive perspective, meaning what you see with the software is what is *placed onto* the board, while other layers are shown from a negative perspective, meaning what you see with the software is what is *removed from* the board. The layers represented in the positive view are the board outline, routed copper, silk screens, solder paste, and assembly information. The layers represented in the negative view are drill holes and soldermasks. Copper plane layers are handled in a special way, as described next.

Fig. 1.17 shows routed layers (top and bottom and an inner, for example) that PCB Editor shows in the positive perspective. The background is black and the traces and pads on each layer are a different color to make it easier to keep track of visually. The drill holes are not shown because, as mentioned already, the drilling process is a distinct step performed at a specific time during the manufacturing process.

Fig. 1.18 shows examples of drill symbols and silk screen representations used by PCB Editor (traces not shown). The *red shapes* (gray in print version) are examples of drill symbols that indicate locations of the drill holes and are used in conjunction with a drill chart (Fig. 1.19), which produces ID numbers for the different drill tools. The white print is the silk screen discussed previously.

Fig. 1.20A shows the soldermask with the patterned holes that allow access to pads, and Fig. 1.20B shows the negative representation used by PCB Editor. Here, the black background is actually the polymer film and the *green circles* (gray in print version) are the holes in the soldermask.

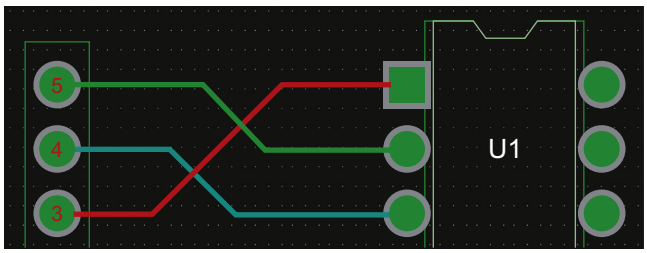

Figure 1.17 Copper in routed layers.

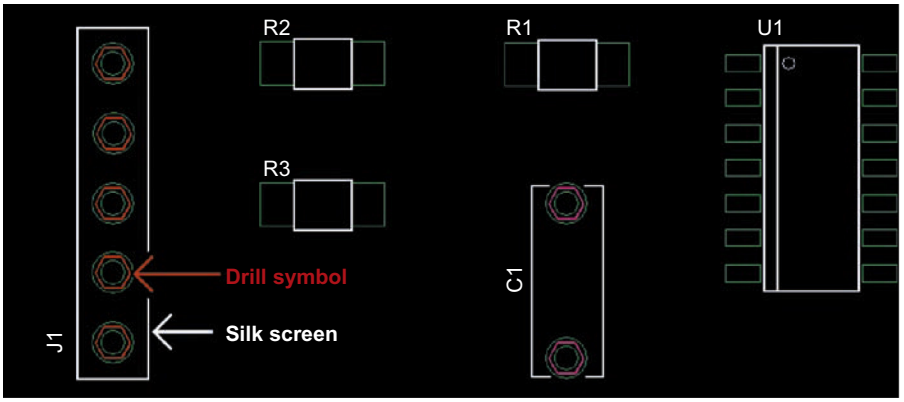

Figure 1.18 Circuit layout with drill symbols and silk screen on a PCB.

Figure 1.19 Drill chart with drill symbols and specifications.

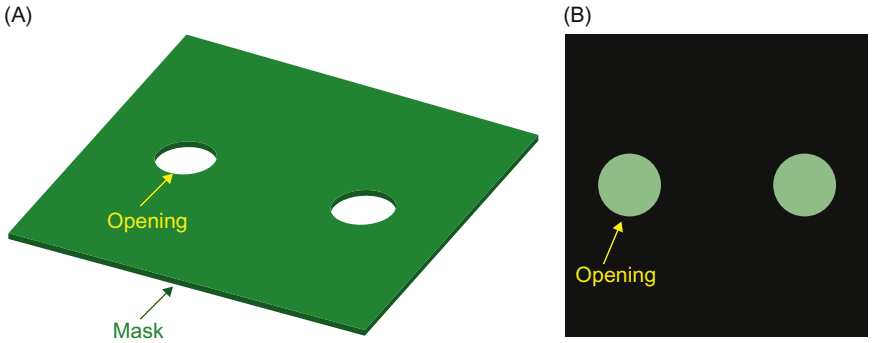

Figure 1.20 Soldermask layer and negative view: (A) soldermask and (B) negative view in PCB Editor.

Plane layers may be processed as negative layers in PCB Editor and are used to generate negative image Gerber files. However, PCB Editor displays plane layers in the positive view. Fig. 1.21A shows a physical copper plane layer with a thermal relief for a pin, Fig. 1.21B shows the negative view, and Fig. 1.21C shows the representation displayed by PCB Editor in "what you see is what you get" mode.

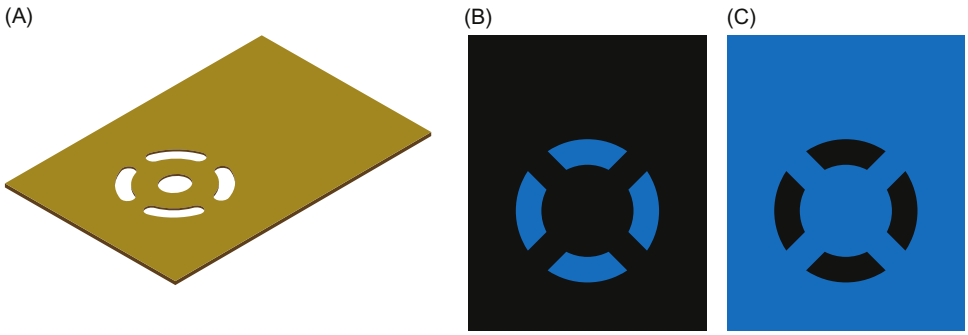

Figure 1.21 Copper in a plane layer: (A) copper plane with thermal relief, (B) negative view as processed, and (C) displayed in WYSIWYG mode. *WYSIWYG*, What you see is what you get.

Design files created by PCB Editor

PCB Editor format files

When you are designing a board, a PCB Editor works with and saves the design in a format that is efficient for the computer. The PCB Editor designed file has a .brd extension. When you are ready to fabricate the board, PCB Editor processes the design and converts it into a format that the photoplotters and CNC machines can use. These files are called *Gerber and drill files*.

Artwork (Gerber) files

Artwork (Gerber) files are created for each of the etch and mask layers discussed previously, and drill files are created for both plated and nonplated holes. PCB Editor generates as many as 30 or so layer files to describe various manufacturing aspects of the PCB. Some examples of these files, their extensions, and their functions are listed in Table 1.1.

These and other files (such as combined format IPC2581) that PCB Editor generates are discussed in greater detail in the next two chapters and in the PCB design examples.

Printed circuit board assembly layers and files

Several layer files generated by PCB Editor are not part of the actual fabrication process. These files are used for automated assembly of a finished board and are mentioned only briefly here. The first layer is the solder-paste layer. It is used to make a contact mask (or *stencil*) for selectively applying solder paste onto the PCB's pads so that components can be reflow soldered to the board. There may be one solder-paste layer for the top side of the board and one for the bottom side, as indicated in Table 1.1. The second layer file is the assembly layer, which contains information for board assemblers as to the part type, its position, and its orientation on the board. As

Table 1.1 PCB project, Gerber and Drill files, their extensions, and their functions.

File name and extension	Function
ProjectName.brd	Main board project file
Assembly_Top.art	Top side assembly
Solderpaste_Top.art	Top side solder paste
Silkscreen_Top.art	Top side silk screen
Soldermask_Top.art	Top side soldermask
TOP.art	Top side copper (usually routing)
INNER1.art	Inner layer 1 (usually routing)
INNER2.art	Inner layer 2 (usually routing)
INNERx.art	Inner layer *x* (usually routing)
PWR.art	Power layer (a plane layer)
GND.art	Ground layer (a plane layer)
BOTTOM.art	Bottom side copper (usually routing)
Soldermask_Bottom.art	Bottom side soldermask
Silkscreen_Bottom.art	Bottom side silk screen
Solderpaste_Bottom.art	Bottom side solder paste
Assembly_Bottom.art	Bottom side assembly
ProjectName.rou	Board outline cutting path
ProjectName.drl	Drill hole data

with the solder-paste layer, there may be one assembly layer for the top side of the board and one for the bottom side. PCB design for the various soldering and assembly processes is discussed in Chapter 5, Introduction to design for manufacturing.

The purpose of this chapter has been to introduce you to the process by which PCBs are manufactured. The purpose of the next chapter is to show you how to use OrCAD PCB Editor to design a board and generate the files needed to manufacture the PCB.